

Application
for
United States Letters Patent

To all whom it may concern:

Be it known that,

Katsuhiko Aisu

have invented certain new and useful improvements in

**SEMICONDUCTOR INTEGRATED CIRCUIT AND AMPLIFIER FOR SUPPRESSING
POP SOUND WHILE MINIMIZING VOLTAGE TRANSITION SETTLING TIME**

of which the following is a full, clear and exact description:

**SEMICONDUCTOR INTEGRATED CIRCUIT AND AMPLIFIER
FOR SUPPRESSING POP SOUND
WHILE MINIMIZING VOLTAGE TRANSITION SETTling TIME**

5 COPYRIGHT NOTICE

A portion of the disclosure of this patent document contains material which is subject to copyright protection. The copyright owner has no objection to the facsimile reproduction by anyone of the patent document or the patent
10 disclosure, as it appears in the Patent and Trademark Office patent file or records, but otherwise reserves all copyright rights whatsoever.

BACKGROUND

15 Field

The present specification relates generally to semiconductor integrated circuits and amplifiers employing a semiconductor integrated circuit for driving an acoustic element, and in particular to semiconductor integrated
20 circuits and such amplifiers capable of reducing a pop sound while minimizing a voltage transition settling time for settling a voltage transition when an operational condition changes.

25 Discussion of the related art

A conventional amplifier driving an acoustic element such as a headphone sometimes generates a strange sound such as a pop sound, when an operational condition changes, such as when electric power is supplied for the first time, a

sleep mode which saves electric power consumption starts or is terminated, etc. Such a pop sound is generally reduced by using a prescribed voltage signal which has rise and decay moderated by a large capacitance (C_{LARGE}) and a plurality of resistances (R_0 , R_1) which have a prescribed decay time constant as discussed in the Japanese Utility Model Patent Publication No.7-22898. Reference signs "M0", "slp", and "out" appearing in the publication represent a MOS transistor, an input signal designating a sleep mode, and an output signal output from a driving amplifier, respectively. Specifically, in order to reduce the pop sound, the output itself is directly moderated. Otherwise, a reference voltage input to the driving amplifier is moderated in order to indirectly moderate the output.

Rising (or decaying) waveforms of such input and output signals "slp" and "out" are exemplified in FIGS. 8A and 8B, and are generally calculated by the following formula, wherein the reference signs "A", "T", "C", and "R" represent a change in a voltage in accordance with a change in an operational condition, time elapsing, capacitance, and a resistance value, respectively:

$$A \times (1 - \exp(-T/(C \times R)))$$

According to such a state of art, however, an inclination of the voltage is sharpest immediately after commencement of charging or discharging a capacitor element as illustrated in FIG. 8B, and thereby the pop sound is likely generated. In order to avoid the pop sound from reaching

a displeasurable level, a high voltage transition settling time, for example, a few seconds, are necessitated in such a state of art. As a result, voltage transition settling time necessarily delays an up and run time for an instrument,
5 when the electric power is supplied for the first time or the like occurs as a problem.

SUMMARY

Accordingly, an object of the present disclosure is
10 to address and resolve such and other problems and provide a new semiconductor integrated circuit.

The above and other objects are achieved by providing a novel semiconductor integrated circuit including a capacitor element, an MOS transistor connected to the
15 capacitor element via its gate, and a constant current generating element which generates a constant current. The preferred embodiment charges the capacitor element with the constant current to create and apply a linearly changing voltage to the gate. The controller controls the MOS
20 transistor to output a smoothly changing current in accordance with the linearly changing voltage.

In another embodiment, a driving amplifier which drives an acoustic element includes such a semiconductor integrated circuit.

25 In yet another embodiment, the driving amplifier includes an inversion operational amplifier having a positive reference input terminal, and the output of the

semiconductor integrated circuit is applied to the positive reference input terminal.

In yet another embodiment, a semiconductor integrated circuit smoothly changes an output of the driving amplifier
5 using the semiconductor integrated circuit when an operational condition changes.

BRIEF DESCRIPTION OF DRAWINGS

A more complete appreciation of the present disclosure
10 and many of the attendant advantages thereof can be more readily understood from the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1A illustrates a circuit employing an N-channel
15 MOS transistor, in accordance with a preferred embodiment of the present disclosure;

FIG. 1B illustrates such a circuit employing a P-channel MOS transistor;

FIG. 2 illustrates V_{gs} - I_d characteristics for such
20 a transistor;

FIG. 3 illustrates an exemplary circuit, according to a preferred embodiment of the present disclosure;

FIGS. 4A to 4F illustrate voltage waveforms appearing at points "A", "B", "out", and "out2", and those of "bpfout"
25 and "bpfout2" appearing after passing through a baseband filter in the circuit of FIG. 3;

FIG. 5 illustrates a circuit of an amplifier driving

an acoustic element, according to an embodiment which employs the semiconductor integrated circuit of FIG. 3;

FIG. 6 illustrates a circuit of an amplifier driving an acoustic element, according to another embodiment which
5 employs such a semiconductor integrated circuit;

FIG. 7 illustrates a conventional circuit for driving an acoustic element;

FIG. 8A illustrates a conventional waveform as an input signal of the conventional circuit of Fig. 7; and

10 FIG. 8B illustrates a conventional waveform as an output signal of the conventional circuit of Fig. 7.

PREFERRED EMBODIMENTS OF THE PRESENT DISCLOSURE

A description of some exemplary embodiments is provided
15 below with reference to the drawings, wherein like reference numerals designate identical or corresponding parts throughout several views.

In particular in FIGS. 1A and 1B, the reference numerals M1 and M14 represent an N-channel MOS transistor and a
20 P-channel MOS transistor, respectively. The reference numerals I0 and I1 represent constant current sources, and the reference numerals CLARGE and CLARGE2 represent large capacitor elements.

A signal rising (or decaying) waveform may be generated
25 in a manner that a linear voltage is initially generated by charging (or discharging) a capacitor element with a constant current and is then applied to an MOS transistor

as a gate and source voltage. The large capacitor element C_{LARGE} , typically arranged outside the IC, may be charged (or discharged) with a drain current flowing from the MOS transistor.

5 As a result, the conventional problem of a sharp inclination can be moderated without unnecessarily prolonging a voltage transition settling time period.

Specifically, as shown in FIG. 1A, when voltages of both ends of the capacitor C_0 are zero volts at the time
10 of $T=0$ (see FIG. 4), the capacitor C_0 is charged with a current flowing from the constant current source I_0 . Since a change in a voltage may be calculated at the point A by the following formula, a linear voltage may be generated:

$$dV/dt = I/C = \text{constant}$$

15 If such a linear voltage is applied to the MOS transistor as a gate and source voltage, a drain current flowing from the MOS transistor smoothly rises and has V_{gs} - I_d characteristics as shown in FIG. 2. Accordingly, the immediate change sharply appearing after the commencement
20 of charging (or discharging) in the conventional circuit can be moderated, and thereby the pop sound may be reduced or sometimes even eliminated.

A first specific embodiment is now described with reference to FIG. 3. Specifically, as shown, a voltage signal
25 "slpb" which is an inversion of the voltage signal "slp" is employed. That is, when the signal slp is in a high level, the signal slpb is in a sleeping level. When the signal slp

is in a low level, the slpb is in an active level. An output terminal "out" is a ground level ("gnd") in a sleeping mode, and a Vref level in an active mode, respectively. The resistances R0 and R1 may be connected to the output terminal
5 out for the purpose of adjusting a rising (and/or decaying) signal waveform. However, it can be omitted or shorted.

According to such a preferred embodiment, a change in a voltage in accordance with a change in an operational condition at each of the nodes A, B, and out appears as shown
10 in FIGS. 4A to 4C, respectively. In particular, the voltage of the output terminal out apparently changes smoothly.

It is also apparent from FIG. 4D when compared with the output out (FIG. 4C) that an output "out2" lacks smoothness at an initial stage of the voltage change. The output out2
15 is conventionally obtained by adjusting the elements of the circuit of FIG. 7 so as to enable its voltage transition settling time to almost correspond to that of the output out.

Further, as shown in FIGS. 4E and 4F, filter output
20 waveforms "bpfout" and "bpfout2" are obtained by having the above-mentioned outputs out and out2, respectively, undergo filtering of a filter (e.g., band pass filter bpf) which only allows a human audible frequency, the latter (i.e. bpfout2) may be larger. Because, a scale of the waveform
25 bpfout2 is a double figure of that of the waveform bpfout. Based on experimentation, the largeness is considered to correlate to that of a strange sound. Specifically, the

larger the scale, the greater the strange sound.

In such a situation, the amplitude of the waveform bpfout can of course be suppressed by prolonging a decay time period. However, the voltage transition settling time
5 period results in becoming intolerably long. Thus, this option is unemployable.

Additional exemplary embodiments are now described with reference to FIGS. 5 and 6. One embodiment may be a headphone amplifier including the semiconductor circuit of
10 FIG. 3, as shown in FIG. 5. The capacitor element CLARGE is, however, externally connected. A driving amplifier is turned ON when an operational condition changes. The output of the driving amplifier can similarly be controlled to change smoothly as mentioned earlier. A signal slp input to an
15 amplifier can preferably be used commonly. It can separately be controlled, however, and still falls within the scope of the present disclosure and the appended claims.

Another embodiment may be a headphone amplifier again including the semiconductor circuit of FIG. 3, as shown in
20 FIG. 6. An output of the driving amplifier may be controlled to be HI-Z (i.e., high impedance) in a sleeping mode. A sleep signal of the semiconductor circuit of FIG. 3 varies when the driving amplifier is in a sleeping mode. Specifically, the driving amplifier is turned OFF when an operational
25 condition changes, as shown in FIG. 6. Thus, a voltage which is output from the driving amplifier is smoothly changed by a circuit (not shown) other than the driving amplifier.

For example, a driving amplifier initially enters into a sleep mode, and the capacitor C_0 is smoothly discharged, and the sleeping mode is realized. Otherwise, the capacitor C_0 is smoothly charged, and the driving amplifier escapes
5 from the sleep mode, and the operational condition is realized. By controlling in such a manner, a pop sound can be suppressed.

The above specific embodiments are illustrative, and many variations can be introduced on these embodiments without departing from the spirit of the disclosure or from
10 the scope of the appended claims. For example, elements and/or features of different illustrative embodiments may be combined with each other and/or substituted for each other within the scope of this disclosure and appended claims.

This specification claims priority under 35 U.S.C.
15 § 119 to Japanese Patent Application No. 2003-017506, filed on January 27, 2003, the entire contents of which are herein incorporated by reference.